

## A MONOLITHIC DC-1.6GHZ DIGITAL ATTENUATOR

J. Bayruns, P. Wallace and N. Scheinberg

ANADIGICS, INC.  
 35 Technology Drive  
 Warren, New Jersey 07060

## ABSTRACT

A 5-bit digital attenuator with integral TTL compatible switch drivers is described. The unit has a 15.5dB attenuation range in 0.5dB increments, 3dB insertion loss, operating frequency range from DC to 1.6GHz, and 1.4:1 input/output VSWR over that frequency range. The unit employs the use of GaAs MESFET integrated circuit technology.

## INTRODUCTION

There are two ways to make a digitally controlled variable attenuator. The first is to use a variable attenuator and control it with a D/A converter. Since an attenuator and DAC, as well as additional control circuitry must be provided, this can be both area and cost intensive (1,2). The second, and most often used way to build a suitable device, is to design it using discreet (digital) stages. The most common method uses contact switches in SPDT form to switch in and out attenuation pads. Although this allows for low insertion losses and high isolation, these units tend to be large in size and slow in switching. Since they have moving parts, they are also prone to wear and tend to be power hungry.

Another method in making these devices is to use solid-state switches in both hybrid and integrated form. Hybrid circuits tend to be large in size and costly to produce. Integrated circuits have the best use of area versus performance, but chip size must be kept small enough, and yield kept high enough, to be cost effective (3).

The purpose of this paper is to describe the design and performance of a GaAs attenuator integrated circuit, which is based on switchable attenuation pads. This design allows for small chip size, fast switching, reduced power dissipation and contains integral TTL compatible switch drivers.

## CIRCUIT DESIGN

Attenuator Section

In order to get away from the use of SPDT switches, a design based on switched resistors is used instead. Because it uses only two variable resistors (as opposed to PI or TEE versions which use three), a bridged-T attenuator circuit is used. Figure 1 shows a bridged-T circuit. When R1 and R2 are picked properly, a varying attenuation is obtained with constant input and output impedance. For example, R1 and R2 are set to one set of values, R1=1.76ohms and R2=1423ohms, to give attenuation=0.3dB, then reset to another set of values, R1=4.82ohms and R2=518ohms to give attenuation=0.8dB. This results in an insertion loss of 0.3dB and an attenuation range of 0.8-0.3=0.5dB. The resistance values are changed using MESFETs as lossy switches (4).

As seen in Figure 1, we use a combination of resistors and FETs to get the values needed for the resistors (R1 & R2). With FET1 on, R1 equals  $r_1$  in parallel with the  $r_{ds}$  of FET1. With FET1 off, R1 equals  $r_1$ . R2 is similar, but in order to keep FET2 from saturating at large power levels, a resistor in series with FET2 was added. As FET2 switches on and off, we obtain the two values for R2. Note that FET1 and FET2 must be switched differentially.

The total attenuator is then composed of five of these stages, each having its own attenuation and insertion loss. For this design, the bits are broken up into 0.5, 1, 2, 4, and 8dB values. The total insertion loss adds up to 3dB.

Switch Driver Section

As stated above, differential control voltages are needed to drive each attenuation stage. Because of design complexity and power dissipation issues, a differential amplifier

approach, shown in Figure 2, is used. A level shifter shifts the incoming clock signal down to the diff amp to facilitate an output swing as wide as possible. Two additional FETs are added to the differential inputs to supply insensitivity to processing variations. Each attenuation stage is driven by one such driver circuit.

## RESULTS

For all measurements shown, the device was mounted in a 10-lead flat package. Figures 3 and 4 show the frequency response for all attenuation values (from 3-18.5dB). As can be seen, the insertion loss is 3dB and maximum attenuation is a little larger than 15.5dB. The 3dB bandwidth is actually  $\gg 2\text{GHz}$ , but the integral and differential linearity of the device is kept below 1/2 LSB only up to 1.6GHz. The attenuator is shown to operate down to 5Hz and is actually able to operate down to DC (the DC offset is 40mV for 0dB attenuation and  $<1\text{mV}$  for 15.5dB attenuation).

Figures 5 and 6 show the minimum to maximum and maximum to minimum switching times, respectively. It can be seen that all switching transients are less than 15nsec. Figure 7 shows the attenuator switching on a 100MHz RF signal. Note that there are not any long switching tail effects noticeable on any of the switching transients.

The chip photograph is shown in Figure 8. The RF attenuator can be seen at the top of the chip (input on the left, output on the right), and switch drivers on the bottom. The control lines and supply lines are located below the switch drivers. The chip size is 1.8mm x 1.8mm. This allows for  $>1000$  chips on a 3" wafer.

The input and output matches into 50ohms were measured to be better than 1.4:1 over the operating frequency range DC-1.6GHz. This can be seen in Figures 9 and 10.

The attenuation was measured for various RF input power levels for every attenuation state. It was defined that the maximum input level was at the point where the attenuation fell by 1 LSB or 0.5dB. This was found to occur at an RF input level of 20dBm.

The chip is supplied by +5V/-7V supplies and draws less than 20mA. The overall schematic is shown in Figure 11. The device performance is summarized in Table 1.

## CONCLUSION

The design and measurement of a 5-bit digital attenuator has been presented. The 15.5dB attenuation range in 0.5dB increments and 3dB insertion loss matches with the measured performance. It has a usable bandwidth from DC

to 1.6GHz and good input and output match over that frequency range (1.4:1 into 50ohms). The performance is typified by its integral and differential linearity ( $<0.25\text{dB}$  @ 1.6GHz and  $<0.1\text{dB}$  below 1.6GHz) and 15nsec RF switching time. The power performance is summarized by its  $<250\text{mW}$  power consumption and 20dBm maximum RF input power level. It has a small chip size ( $<4\text{mm}$  square) and has TTL compatible control inputs.

TABLE I

### Device Characteristics

#### DC Characteristics

|               |                                  |
|---------------|----------------------------------|
| Atten. Range: | 15.5dB+0.1dB in 0.5dB increments |
| Min. Atten:   | -3.0dB+0.25dB                    |
| Max. Atten:   | -18.5+0.25dB                     |

#### AC Characteristics

|                      |                         |
|----------------------|-------------------------|
| -3dB Frequency:      | >5GHz                   |
| -0.5dB Frequency:    | 1.6GHz                  |
| Input/Output VSWR:   | <1.4:1 (from DC-1.6GHz) |
| Atten. Flatness:     | <+0.1dB                 |
| RF Switching Time:   | <15nsec (min. to max.)  |
| Max. RF Input Power: | 20dBm                   |

#### Supply Characteristics

|                  |          |
|------------------|----------|
| Supply Voltages: | +5V, -7V |
| Supply Currents: | +20mA    |
| Supply Power:    | <250mW   |

## REFERENCES

- (1) Y. Tajima, et al., "GaAs Monolithic Wideband (2-18 GHz) Variable Attenuators," 1982 IEEE MTT-S Digest, pp. 479-481.
- (2) G. S. Barta, et al., "Surface-Mounted GaAs Active Splitter and Attenuator MMICs Used in a 1-10 GHz Leveling Loop," IEEE Trans. Microwave Theory Tech., Vol. MTT-34, No. 12, Dec. 1986.
- (3) R. Gupta, et al., "A 0.05 to 14 GHz MMIC 5-Bit Digital Attenuator," 1987 IEEE GaAs IC Symposium, pp. 231-234.
- (4) Y. Ayasli, "Microwave Switching with GaAs FETs," Microwave Journal, Nov. 1982, pp. 61-64, 66, 68, 70-72, 74.

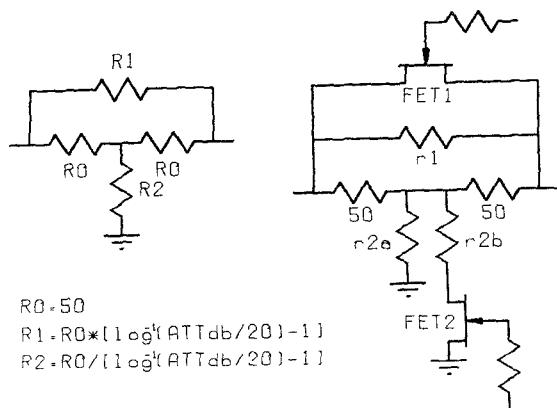


Figure 1. Bridged-T Attenuator Section

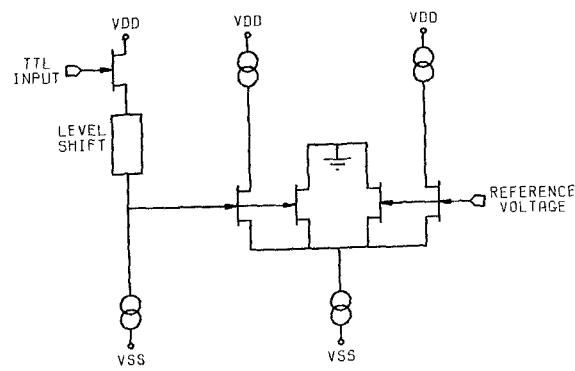


Figure 2. Switch Driver Schematic

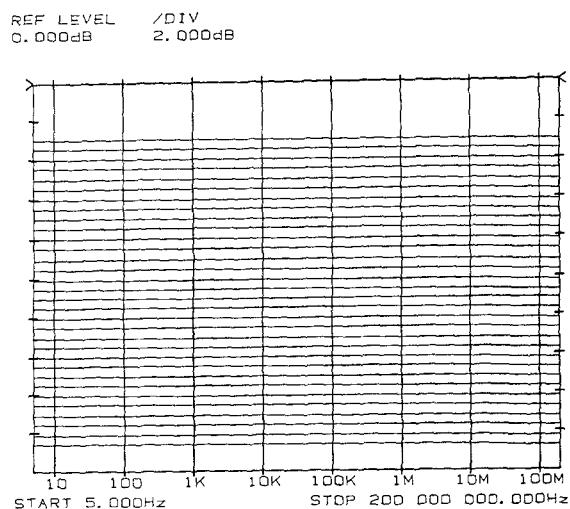


Figure 3. 5Hz to 200MHz Frequency Response All 32 Attenuation Levels

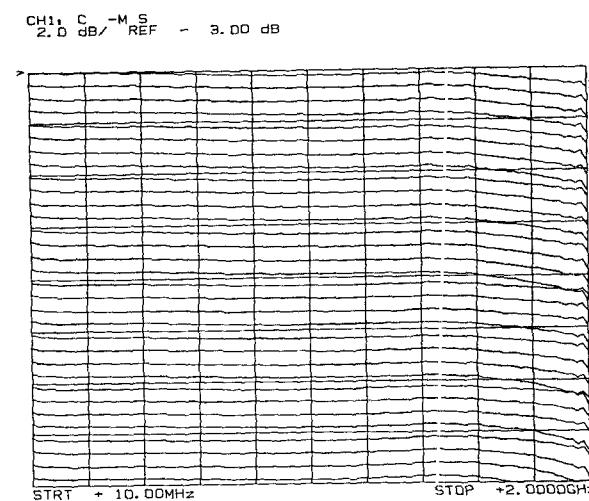


Figure 4. 10MHz to 2GHz Frequency Response All 32 Attenuation Levels

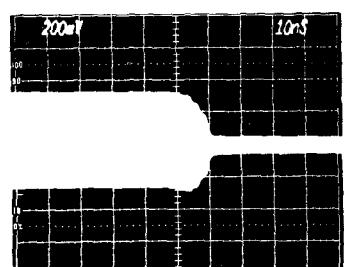


Figure 5. Minimum to Maximum Attenuation Switching Transient

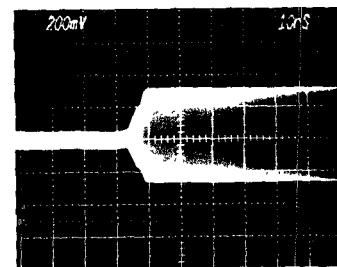


Figure 6. Maximum to Minimum Attenuation Switching Transient

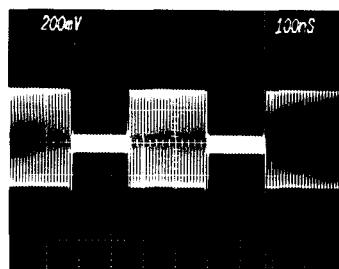


Figure 7. Long Switching Transient

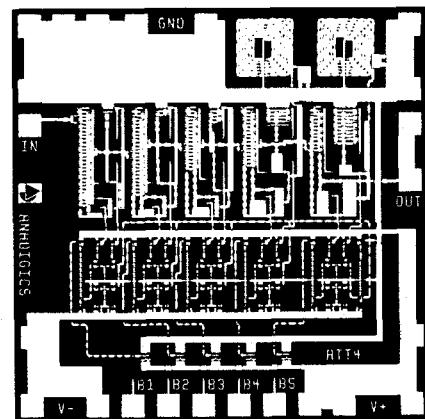


Figure 8. Chip Photograph

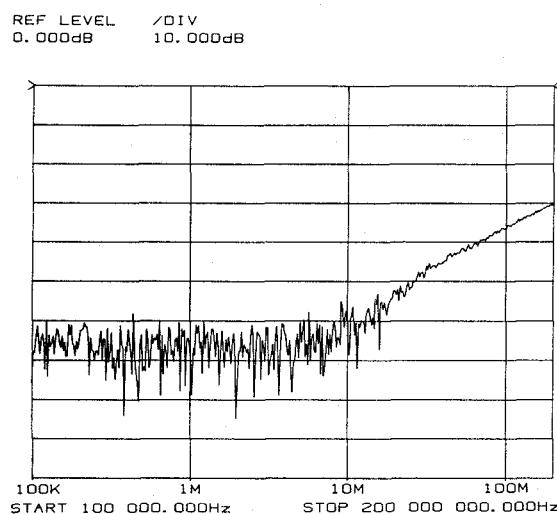


Figure 9. S11 & S22 -100KHz to 200MHz

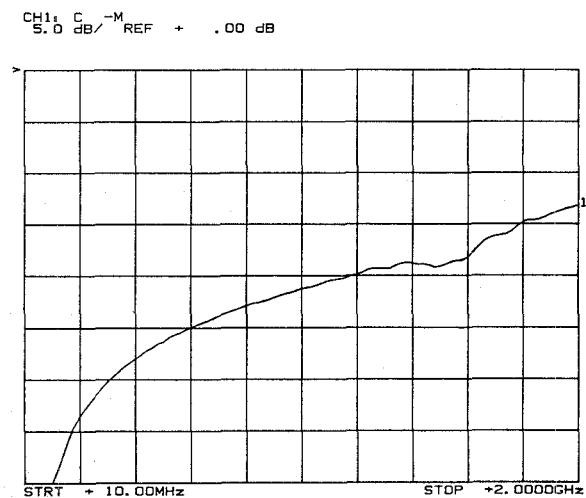


Figure 10. S11 & S22 -10MHz to 2GHz

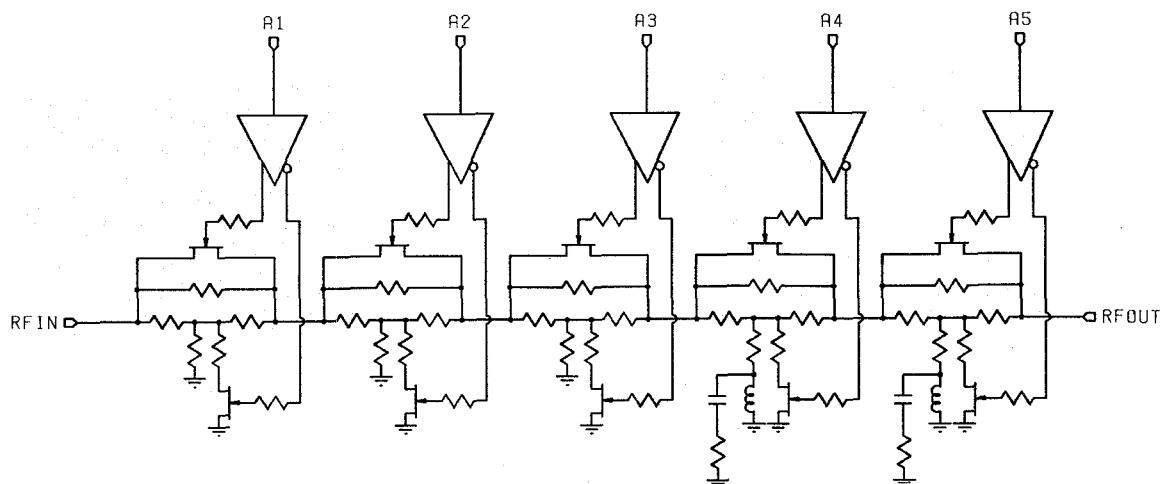


Figure 11. Total Device Schematic